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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/772,493	01/30/2001	David W. Duemler	D6570-00003	1363
8933	7590	07/02/2004	EXAMINER	
DUANE MORRIS, LLP IP DEPARTMENT ONE LIBERTY PLACE PHILADELPHIA, PA 19103-7396				NGUYEN, LE V
ART UNIT		PAPER NUMBER		
		2174		

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/772,493	DUEMLER, DAVID W. <i>[Signature]</i>
	Examiner	Art Unit
	Le Nguyen	2174

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 07 May 2004.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-22 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. This communication is responsive to Amendment A, filed 4/7/04.
2. Claims 1-22 are pending in this application; and, claims 1, 9, 17 and 20 are independent claims. This action is made Final.
3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5, 8, 9, 16, 17 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by McLaughlin.

As per claim 1, McLaughlin teaches a method of programming a programmable logic controller, the programmable logic controller including a plurality of inputs and a plurality of outputs, the programmable logic controller directing a process through output signals at the outputs in response to input signals at the inputs (figs. 2, 10-11 and 13-23; col. 6, lines 10-34; col. 7, lines 15-20 and 57-62; col. 13, lines 20-35; col. 14, lines 15-17; col. 18, lines 3-20; col. 23, lines 45-52), comprising the steps of:

displaying to a user on a monitor a graphical data entry user interface for a plurality of sequential steps the graphical data entry user interface representing respective inputs to be monitored by the programmable logic controller at each of the sequential steps and respective outputs to be initiated by the programmable logic controller at respective ones of the sequential steps (figs. 13-23; col. 13, lines 20-35; col. 14, lines 15-17; col. 18, lines 3-20);

receiving, via the graphical data entry user interface, an identification of at least one input selected by the user to be monitored for at least one of the sequential steps and an identification of at least one output selected by the user to be initiated for the at least one of the sequential steps (fig. 22; col. 18, lines 3-20; *the I/O module selection is indicated as activated for slot number 002 by the 16 / 16 BLOCK module type displayed on configuration screen 2200, and the INPUT STATE of channel number 33 is indicated as "ON" while OUTPUT STATE of channel number 33 is indicated as "OFF"*);

converting the identification of the at least one input selected by the user into an input control data table, the input control data table including a plurality of input control data elements, each of the input control data elements corresponding to a respective one of the plurality of sequential steps, a respective one of the input control data elements representing the at least one input selected by the user (fig. 2; col. 6, lines 10-34); and

converting the identification of the at least one output selected by the user into an output data table, the output data table including a plurality of output data elements, each of the output data elements corresponding to a respective one of the plurality of sequential steps, a respective one of the output data elements representing the at least one output selected by the user (fig. 2; col. 6, lines 10-34).

As per claim 5, the McLaughlin reference teaches a method of programming a programmable logic controller, the programmable logic controller including a plurality of inputs and a plurality of outputs, the programmable logic controller directing a process through output signals at the outputs in response to input signals at the inputs wherein the input control data element includes a plurality of bits and a subset of the plurality of bits represents individual inputs of the programmable logic controller (col. 6, lines 10-34).

As per claim 8, the McLaughlin reference teaches a method of programming a programmable logic controller, the programmable logic controller including a plurality of inputs and a plurality of outputs, the programmable logic controller directing a process through output signals at the outputs in response to input signals at the inputs wherein the output data element includes a plurality of bits and a subset of the plurality of bits represents individual outputs of the programmable logic controller (col. 6, lines 10-34).

Claims 9, 17 and 22 are individually similar in scope to claim 1 and are therefore rejected under similar rationale.

Claim 16 is similar in scope to claim 8 and is therefore rejected under similar rationale.

Claim Rejections - 35 USC § 103

5. Claims 2-4, 10-13, 18, 19, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over McLaughlin in view of Coleman et al. (“Coleman”).

As per claim 2, although McLaughlin teaches a method of programming a programmable logic controller, the programmable logic controller including a plurality of inputs and a plurality of outputs, the programmable logic controller directing a process through output signals at the

outputs in response to input signals at the inputs comprising invoking a timer enable command with timer value when a condition of a step among a plurality of sequential steps is met (col. 7, lines 11-14), McLaughlin does not explicitly disclose the timer enable command and timer value being options on the graphical data entry user interface. Coleman teaches a method of programming a programmable logic controller wherein the graphical data entry user interface includes a timer enable command option for each of the plurality of sequential steps and a timer value option for each of the plurality of sequential steps (figs. 3 and 8; col. 1, lines 50-65; col. 3, lines 45-56; col. 4, lines 17-30 and lines 53-56). Therefore, it would have been obvious to an artisan at the time of the invention to include Coleman's teaching of a graphical data entry user interface that includes a timer enable command option for each of the plurality of sequential steps and a timer value option for each of the plurality of sequential steps to McLaughlin's teaching of invoking a timer enable command with timer value when a condition of a step among a plurality of sequential steps is met in order to provide greater flexibility to the operator and increasing the usefulness of machine cycle time monitoring.

As per claim 3, the modified McLaughlin teaches a method of programming a programmable logic controller, the programmable logic controller including a plurality of inputs and a plurality of outputs, the programmable logic controller directing a process through output signals at the outputs in response to input signals at the inputs, comprising the steps of:

receiving, via the graphical data entry user interface, a selection by the user of a timer enable command for at least one of the plurality of sequential steps (Coleman: fig. 3, col. 4, line 53 through col. 5, line 4; *an operator enables a timer command and controls which items are included*);

receiving via the graphical data entry user interface, a selection by the user of a timer value for said one of the plurality of sequential steps (Coleman: fig. 3, col. 4, line 53 through col. 5, line 4; *an operator enters a timer value, i.e. the amount of time, in seconds, that a particular event of the process should take to complete*); and

creating a timer value data table including at least one timer value data element, the timer value data element representing the timer value wherein a respective one of the input control data elements represents the timer enable command for the one of the sequential steps (Coleman: fig. 3, col. 4, line 53 through col. 5, line 4; McLaughlin: col. 6, lines 10-34).

As per claim 4, the modified McLaughlin teaches a method of programming a programmable logic controller, the programmable logic controller including a plurality of inputs and a plurality of outputs, the programmable logic controller directing a process through output signals at the outputs in response to input signals at the inputs wherein the input control data element includes a plurality of bits, a subset of the plurality of bits representing individual inputs of the programmable logic controller and at least a remaining one of the plurality of bits representing the timer enable command (McLaughlin: col. 6, lines 10-34).

Claims 10, 18 and 21 are individually similar in scope to claim 2 and are therefore rejected under similar rationale.

Claims 11, 19 and 22 are individually similar in scope to claim 1 and are therefore rejected under similar rationale.

Claim 12 is similar in scope to claim 3 and is therefore rejected under similar rationale.

Claim 13 is similar in scope to claim 5 and is therefore rejected under similar rationale.

6. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over McLaughlin.

As per claim 6, although McLaughlin teaches a method of programming a programmable logic controller, the programmable logic controller including a plurality of inputs and a plurality of outputs, the programmable logic controller directing a process through output signals at the outputs in response to input signals at the inputs comprising displaying to a user on a monitor a graphical data entry user interface (figs. 13-23; col. 13, lines 20-35; col. 14, lines 15-17; col. 18, lines 3-20), McLaughlin does not explicitly disclose the graphical data entry user interface being a check grid. Official Notice is taken that the use of check grids are well known in the art. Therefore, it would have been obvious to an artisan at the time of the invention to include the use of a graphical data entry user interface being a check grid to McLaughlin's graphical data entry user interface in order to provide users with another method of organizing data.

Claim 14 is similar in scope to claim 6 and is therefore rejected under similar rationale.

7. Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over McLaughlin in view of Gates et al. ("Gates").

As per claim 7, McLaughlin teaches a method of programming a programmable logic controller, the programmable logic controller including a plurality of inputs and a plurality of outputs, the programmable logic controller directing a process through output signals at the outputs in response to input signals at the inputs comprising the step of downloading a virtual rack module (Abstract), McLaughlin does not explicitly disclose downloading an input control data table and the output data table to the PLC. Gates teaches downloading an input control data table and the output data table (fig. 2; i.e. *the commands which are sent to communications task*

47 for handling are Rung Link which is generated by compiler task 37 when a modified rung has been recompiled, Rung Upload which is generated by editor task 35 when a particular rung in the ladder is to be modified; Data Table Upload and Data Table Download which are generated by housekeeping task 38 to upload and download a data table in RAM 87 which is used to store the status of each data point controlled by the system; Block Read Data Table and Block Write Data Table which are generated by editor task 35 to read and write rung information of the ladder program stored in RAM 85; Read File Name and Write File Name generated by editor task 35 to read and write the file name of the ladder program in RAM 85; and Remove Forces generated by editor task 35 to remove all input/output forcing rungs whenever a ladder is attached or detached). Therefore, it would have been obvious to an artisan at the time of the invention to include Gates' downloading an input control data table and the output data table to McLaughlin's downloading a virtual rack module so that an input control data table and an output data table on a remote computer may be transferred at user's request.

Claim 15 is similar in scope to claim 7 and is therefore rejected under similar rationale.

Response to Arguments

8. Applicant's arguments, see third paragraph of page 21, filed 4/7/04, with respect to the rejection(s) of claim(s) 1-22 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art reference(s).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquires

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Lê whose telephone number is (703) 305-7601. The examiner can normally be reached on Monday - Friday from 5:30 am to 2:00 pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kristine Kincaid, can be reached on (703) 308-0640.

The fax numbers for the organization where this application or proceeding is assigned are as follows:

(703) 872-9306 [Official Communication]

Art Unit: 2174

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

LVN
Patent Examiner
June 22, 2004

Kristine Kincaid
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SUPERVISORY PATENT EXAMINER
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